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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/728,189	12/01/2000	Stephen J. Battersby	PHB 34,424	4514

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER
AKKAPEDDI, PRASAD R

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/728,189	BATTERSBY ET AL.	
	Examiner	Art Unit	
	Prasad R Akkapeddi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagisawa (U.S.Patent No. 4,759,610) (applicant's cited reference).

As to claims 1-3: Yanagisawa discloses an active matrix display with a transistor over the substrate (11), having an insulated-gate staggered structure having substantially coplanar source and drain regions and a gate region (Fig. 7), a gate insulator (23) and a capacitor (Col. 3, line 62) associated with the transistor and lying adjacent the transistor, the capacitor comprising a stacked structure of two electrodes (28,12) separated by a capacitor dielectric (29), wherein the gate insulator comprises a first inorganic layer (23) and a second (25), polymer (Col. 5, lines 11-17), of which layers only the polymer (25) extends to the capacitor (as can be seen in Fig. 7). *Yanagisawa does disclose that the source and drain regions on the substrate (16) (see the response to arguments below).*

As to claim 4: Yanagisawa discloses a polyimide type film (Col. 5, line 17) and the transistor is a top gate transistor with gate electrode (24) on the semiconductor film (22). Yanagisawa also discloses a liquid crystal display comprising a plurality of pixels (TFT array) provided over a transistor substrate (16) with each pixel comprising a respective transistor and capacitor, and in (Col. 4, lines 17-53) discloses the relationship between the thickness of the cell that includes the thickness of the layers and the time constant.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa in view of Jang (U.S.Patent No. 5,734,449).

As to claims 5-9: Although Yanagisawa discloses a liquid crystal display having a top gate transistor and storage capacitance, first inorganic layer, a second polyimide layer, Yanagisawa does not explicitly disclose the relationship between the capacitance and the thicknesses of the insulating layers and their permittivity constants. Jang on the other hand, in disclosing a similar liquid crystal display device, discloses the relationship between the storage capacitance, liquid crystal material capacitance, thicknesses of the layers and the permittivity constants of the layers in (Col. 3, lines 1-33). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the relationships between the capacitances, thicknesses and the permittivity constants as disclosed by Jang to the display device disclosed by Yanagisawa to enhance aperture efficiency and to increase the brightness of the display.

As to claims 10-12: Although Yanagisawa discloses an active matrix display device with a transistor over the substrate (11), having an insulated-gate staggered structure having substantially coplanar source and drain regions and a gate region (Fig. 7), a gate insulator (23) and a capacitor (Col. 3, line 62) associated with the transistor and lying adjacent the transistor, the capacitor

comprising a stacked structure of two electrodes (28,12) separated by a capacitor dielectric (29), wherein the gate insulator comprises a first inorganic layer (23) and a second (25) and in (Col. 5, lines 22-25) discloses that these layers can be formed by normal pressure (non-vacuum) or low pressure (vacuum) deposition techniques. In Fig. 7 Yanagisawa discloses that the first layer (23) is removed from areas corresponding to the capacitors and the second layer (25) extends to the areas extends to the areas corresponding to the capacitors and the relationship between the thicknesses of the layers and the capcitances and the time constant, Yanagisawa does not explicitly disclose the method of manufacturing such a device. Jang on the other hand, discloses a method of manufacturing such a liquid crystal display device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the method of manufacturing the device and the relationships between the capacitances, thicknesses and the permittivity constants as disclosed by Jang to the display device disclosed by Yanagisawa as a way to manufacture the device.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa in view of Jeong (U.S.Patent No. 6,137,551).

a. As to claim 13: Yanagisawa does not disclose that the gate insulator and the first inorganic layer are patterned using the same mask to define a semiconductor island. Jeong on the other hand, in disclosing a liquid crystal display discloses a gate insulating layer (52) and a first insulating layer (54) and

patterning the gate insulator using the insulating layer (54) as a mask (col. 6, lines 31-44). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the structure disclosed by Jeong to the device of Yanagisawa to enhance the aperture ratio without introducing complicated processes.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 6, 10 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Please note that the claim language in the instant claims does not contain the feature that the source and drain regions are ***'directly'*** on the substrate. It just recites that they are on a substrate. Hence the teachings of Yanagisawa are applicable, when one interprets the claim language in a broad sense.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R Akkapeddi whose telephone number is 703-305-4767. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on 703-305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0530.

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July 3, 2003

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800